A Remark on "A Variable Length Shift Register"

Allan Gottlieb[1]

Courant Institute, N.Y.U.
251 Mercer Street
New York, N.Y. 10012

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ABSTRACT

We note that the systolic queue of Guibas and Liang can be used to implement a varying length shift register and is also useful for shared memory multiprocessors.

Danielson [83] introduces a VLSI implementation of a variable-length shift-register. In this short note we observe that the VLSI systolic queue of Guibas and Liang [82] can also be used for this purpose.

Guibas and Liang describe the systolic queue in detail; here we give a rough sketch. As indicated in figure 1, the circuit is a ladder-like structure in which data items enter the bottom of the IN column and begin shifting up. If the adjacent cell in the OUT column is empty, the item shifts horizontally instead of up; data in the out column shift down whenever an item is removed from the bottom.

The systolic queue satisfies two important properties. First, all logic is distributed so that no long signal wires are needed. Second, in contrast with a simpler one column "silo", an insert is possible whenever the queue is not full and a delete is possible whenever the queue is not empty.

To implement a varying length shift register, one simply begins removing items k cycles after they start to enter, where k is the delay currently desired.

Another application of the systolic queue structure can be found in Snir and Solworth [84] where a third SHUTE column is added (see figure 2). In this application the queue is used for the output ports of a buffered packet switched network connecting multiple processors to multiple memory modules. This network has the additional property that requests to the same memory location are "combined": If an item moving up IN matches the

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adjacent OUT item (i.e. if the referenced addresses are the same), the former item moves to SHUTE, which shifts down in synchrony with OUT. Hence the two matching items leave their respective queues simultaneously and thus arrive together at the combining unit (not shown in figure 2).

References

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"A Variable-Length Shift Register", *IEEE Trans* **C-32**, pp. 1067-1069, 1983.

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"Systolic Stacks, Queues and Counters", in *Proc. Conf. Advanced Research VLSI*, January, 1982.

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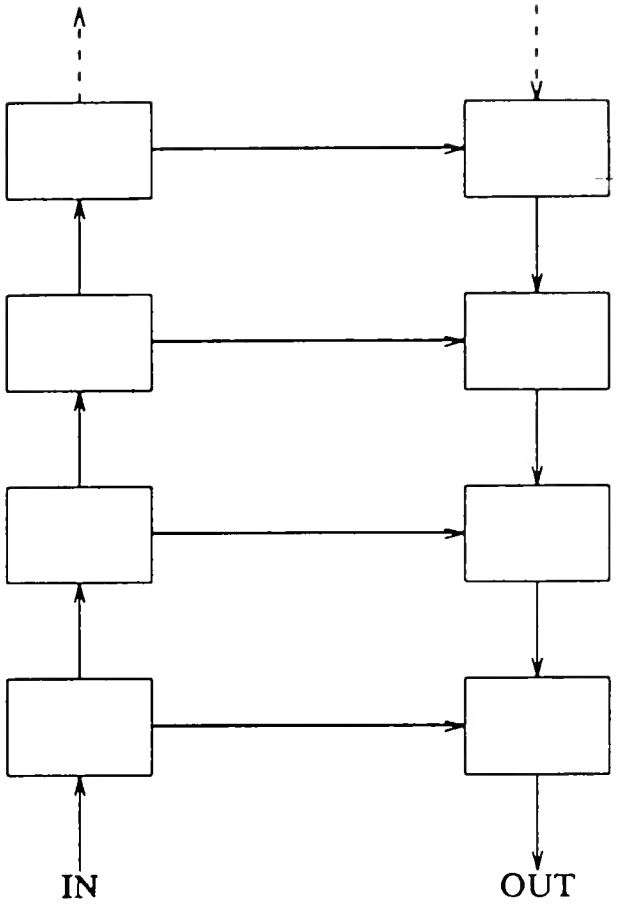

Figure 1. Guibas-Liang systolic queue.

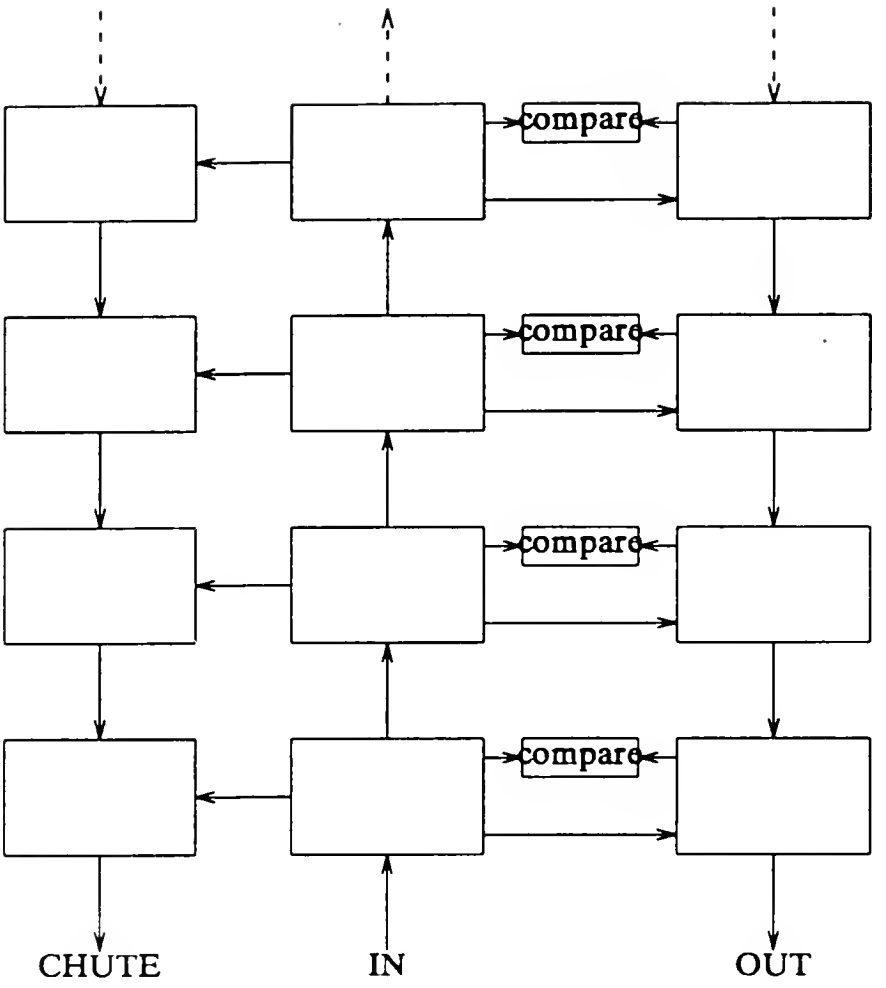

Figure 2. Snir-Solworth extended systolic queue.